3 Phase BLDC Motor Pre-Driver AM6807

The AM6807 is developed to drive 3 phase BLDC. Package material is Pb-Free for purpose of environmental protection.

● Applications

High power BLDC

● Features

1) Pre-driver for MOS-FET driving Circuits.
2) Built in charge pump.
3) Built in FG Amp, hys Amp.
4) Built in Current Limit.
5) PWM drive.
6) Built-in Forward /Reverse Switching
7) Built-inDirect PWM Mode Control Circuits.
8) Under Voltage protection.
9) Short brake mode.
10) Non-overlap design between Hi/Low side motor.

● Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	36	V
Pin Input voltage	V_{in}	VREG	V
Power dissipation	Pd	1.7*	W
Operate temperature range	T_{opr}	-10～＋75	℃
Storage temperature range	T_{stg}	-40～＋150	℃

*70mm×70mm×1.6mm glass epoxy board.

*Reducing in done at 13.6mW/℃ for operating above Ta = 25℃.

**Do not exceed Pd ASO and Tj = 150℃.

● Recommended operating conditions

(Set the power supply voltage taking allowable dissipation into considering)

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage range	Vcc		16~28		V

● Electrical Characteristics

(Unless otherwise specified, Ta = 25℃, VCC = 25.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total						
Circuit current	I_{CC}	13.5	18.07	22.5	mA	
VREG voltage	VREG	5.4	5.9	6.4	V	IVREG=-1mA
HALL AMP						
Input bias current	I_{HA}	-3.0	-0.7	—	μA	
In-phase input voltage Range	V_{HAR}	1.0	—	4.4	V	
Minimum input level	V_{INH}	50	—	—	mV_{PP}	
Hysteresis level	V_{HYS}	10	20	30	mV	
PWM						
Output High voltage	V_{HPCfe}	3.8	4.3	4.8	V	
Output Low voltage	V_{LPCfe}	1.9	2.3	2.7	V	
Oscillation frequency (reference)	F_{Cfe}	17	20	25	kHz	Rfe=45kΩ Cfe=100pF
Pref input current H	I_{PrefH}	—	0.05	1	μA	
Pref input current L	I_{PrefL}	-1	0	—	μA	
FG Amp						
Input bias current	IbFG	-1	—	1	μA	
Input offset voltage	VbFG	-10	—	10	mV	
Output High voltage	VHFG	4.5	5.0	—	V	IHFGOUT=-2mA
Output Low voltage	VLFG	—	1.0	1.5	V	ILFGOUT=2mA
FGsout Low voltage	VLFGS	—	0.1	0.3	V	ILFGSOUT=3mA
Open loop gain	GVFG	45	54	—	dB	
Bias voltage	VbiasFG	2.7	3.0	3.3	V	
Hysteresis	Vhys	100	180	250	mV	

This product is not designed for protection against radioactive rays.

● Electrical Characteristics

(Unless otherwise specified, Ta = 25℃, VCC = 25.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
ACC, DEC						
ACC input current H	I_{ACCH}	—	0	1	μA	ACC=5V
ACC input current L	I_{ACCL}	-3.0	-0.5	—	μA	ACC=0V
DEC input current H	I_{DECH}	—	0	1	μA	DEC=5V
DEC input current L	I_{DECL}	-3.0	-0.5	—	μA	DEC=0V
Acceleration current	Iss	147	210	273	μA	RCP=13.5kΩ
Deceleration current	Iso	-268	-220	-154	μA	RCP=13.5kΩ
ACC input High level	VIHACC	2.0	—	Vreg	V	
ACC input Low level	VILACC	0.0	—	0.8	V	
DEC input High level	VIHDEC	2.0	—	Vreg	V	
DEC input Low level	VILDEC	0.0	—	0.8	V	
Current Limit						
Current detect voltage	V_{CL}	0.373	0.415	0.456	V	
UPPER OUTPUT						
Upper voltage	VHG	V_{CC}+6	V_{CC}+7	V_{CC}+8	V	
Pull down Resistance	R_{HO}	70	100	130	KΩ	
LOWER OUTPUT						
Low voltage	VLG	10	11	12	V	
Pull up Resistance	R_{LU}	14	20	26	KΩ	
Charge pump						
Oscillation frequency	F_{OSC}	147	210	273	KHz	OSC=100pF
Charge pump voltage	V_G	V_{CC}+6	V_{CC}+7	V_{CC}+8	V	

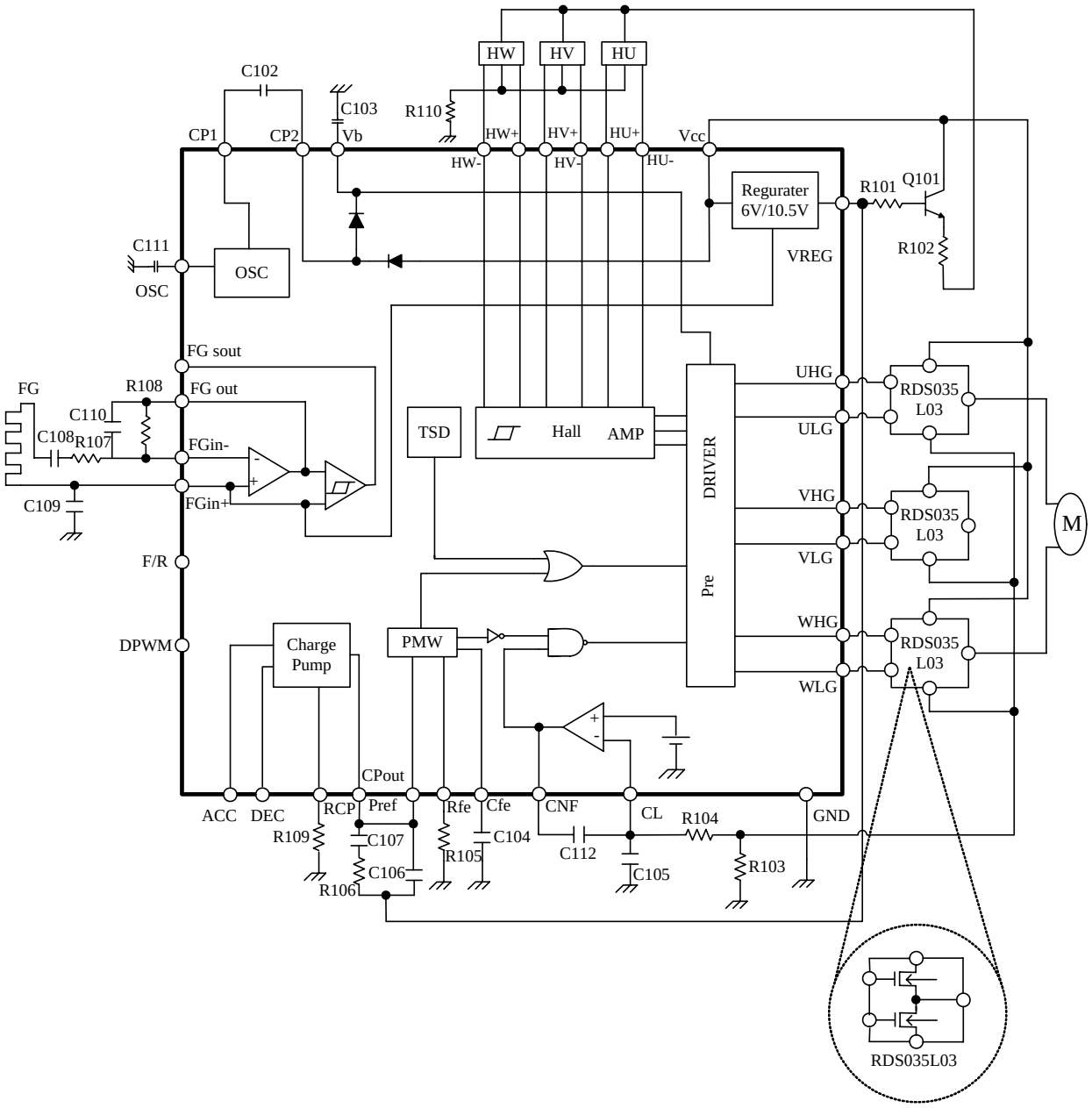
This product is not designed for protection against radioactive rays.

● Electrical Characteristics

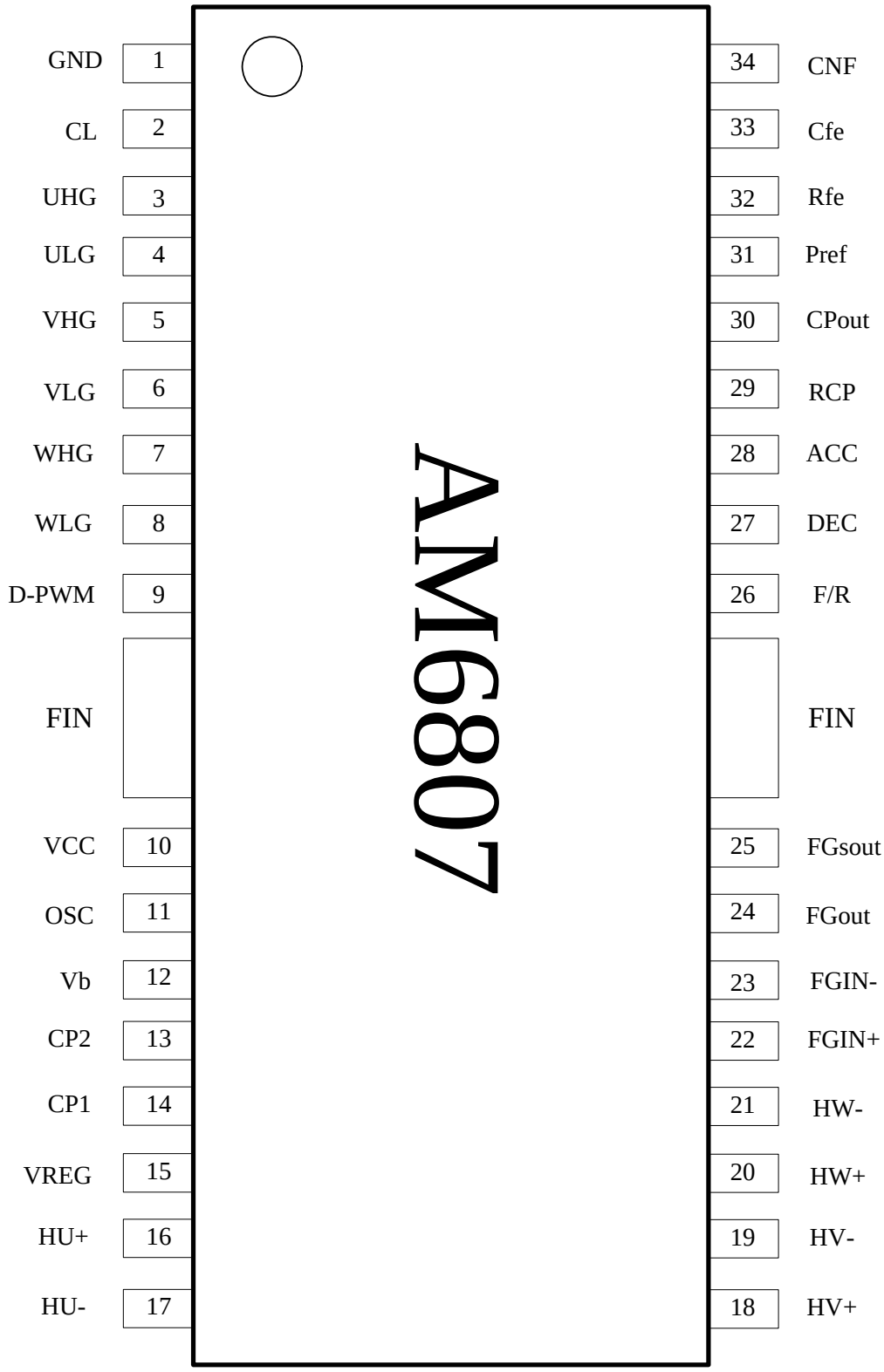
(Unless otherwise specified, Ta = 25℃, VCC = 25.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Under Voltage Detection						
Detecting Voltage	Vdet	16.6	18.44	20.3	V	
Hysteresis	Vhsy1	200	400	600	mV	
D-PWM						
D-PWM frequency (reference)	$F_{D\text{-}PWM}$	—	—	50	kHz	
D-PWM input high level	$V_{IH\ D\text{-}PWM}$	2.0	—	Vreg	V	
D-PWM input low level	$V_{IL\ D\text{-}PWM}$	0.0	—	0.8	V	
D-PWM input current H	I_{DPWMH}	—	0	1	μA	
D-PWM input current L	I_{DPWML}	-3	-0.5	—	μA	
F/R						
F/R input high level	$V_{IH\ F/R}$	2.0	—	5.0	V	
F/R input low level	$V_{IL\ F/R}$	0.0	—	0.8	V	
F/R input current H	$I_{F/R\ H}$	30	60	90	μA	
F/R input current L	$I_{F/R\ L}$	-10	0	10	μA	

Block Diagram



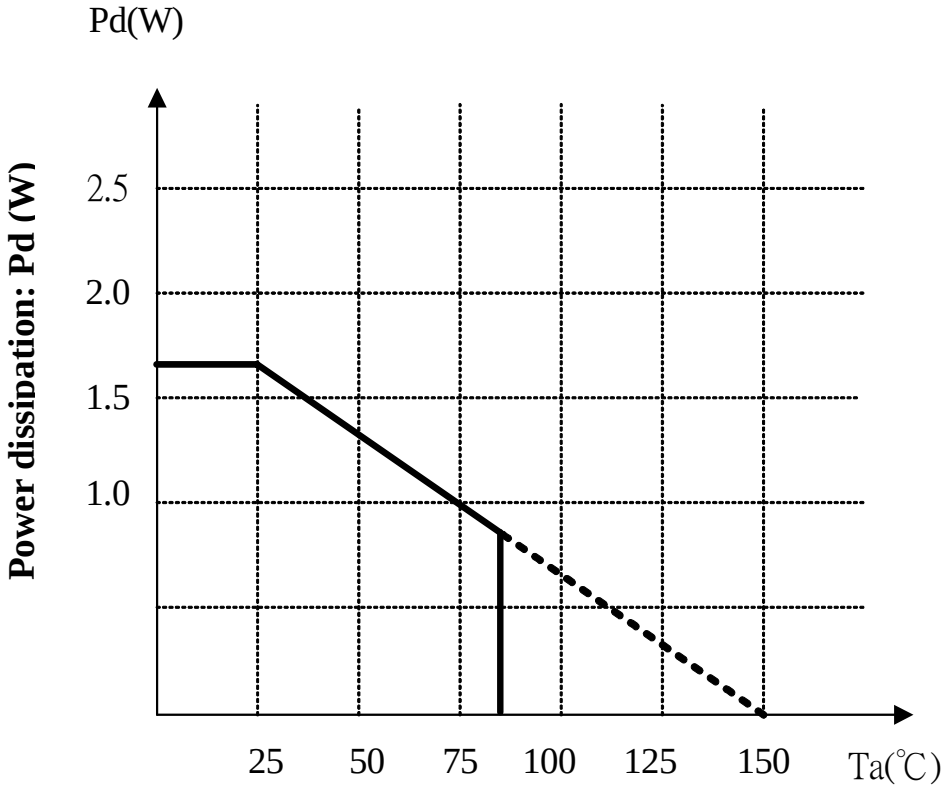
Pin configuration



Pin Description

PIN No	Pin Name	Function
1	GND	GND pin
2	CL	Current limit pin
3	UHG	FET gate pin for phase U upper side
4	ULG	FET gate pin for phase U lower side
5	VHG	FET gate pin for phase V upper side
6	VLG	FET gate pin for phase V lower side
7	WHG	FET gate pin for phase W upper side
8	WLG	FET gate pin for phase W lower side
9	D-PWM	Direct PWM Control Pin
10	Vcc	Power supply for signal division
11	OSC	Capacitor connection pin for oscillator
12	Vb	Capacitor connection pin for Booster
13	CP2	Capacitor pin 2 for Booster
14	CP1	Capacitor pin 1 for Booster
15	VREG	VREG pin
16	HU+	Positive input pin for Hall Amp U
17	HU-	Negative input pin for Hall Amp U
18	HV+	Positive input pin for Hall Amp V
19	HV-	Negative input pin for Hall Amp V
20	HW+	Positive input pin for Hall Amp W
21	HW-	Negative input pin for Hall Amp W
22	FGin+	Positive input pin for FG Amp
23	FGin-	Negative input pin for FG Amp
24	FGout	Output pin for FG Amp
25	FGsout	Symmetric output pin for FG Amp
26	F/R	Forward / Reverse Control Pin
27	DEC	Deceleration signal input pin
28	ACC	Acceleration signal input pin
29	RCP	CPout current control pin
30	CPout	Charge Pump output pin
31	Pref	Signal of PWM control input pin
32	Rfe	Cfe current control pin
33	Cfe	PWM frequency control pin
34	CNF	Phase compensation pin

- **Power dissipation curve:**



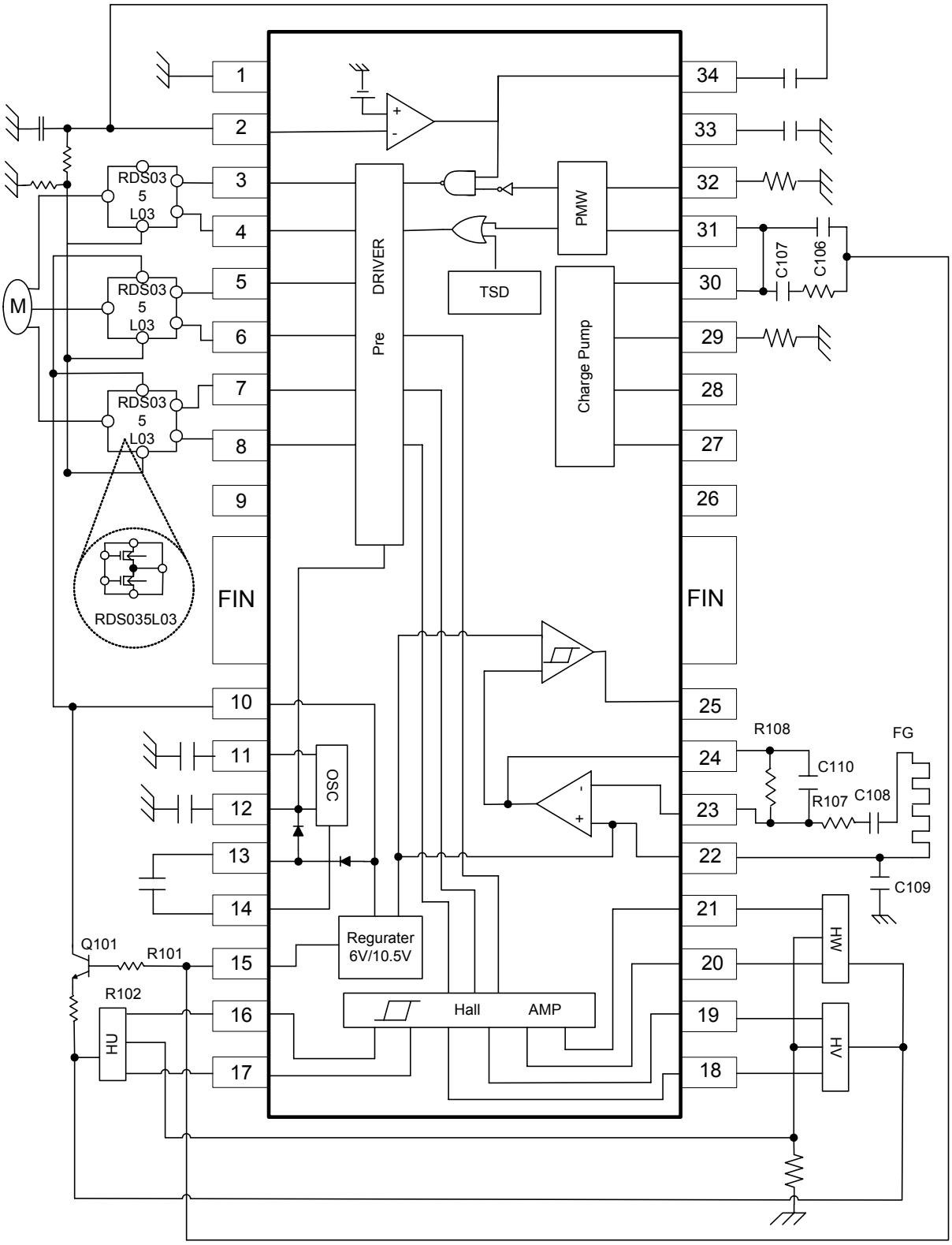
Ambient temperature : Ta (℃)

*70mm×70mm×1.6mm glass epoxy board.

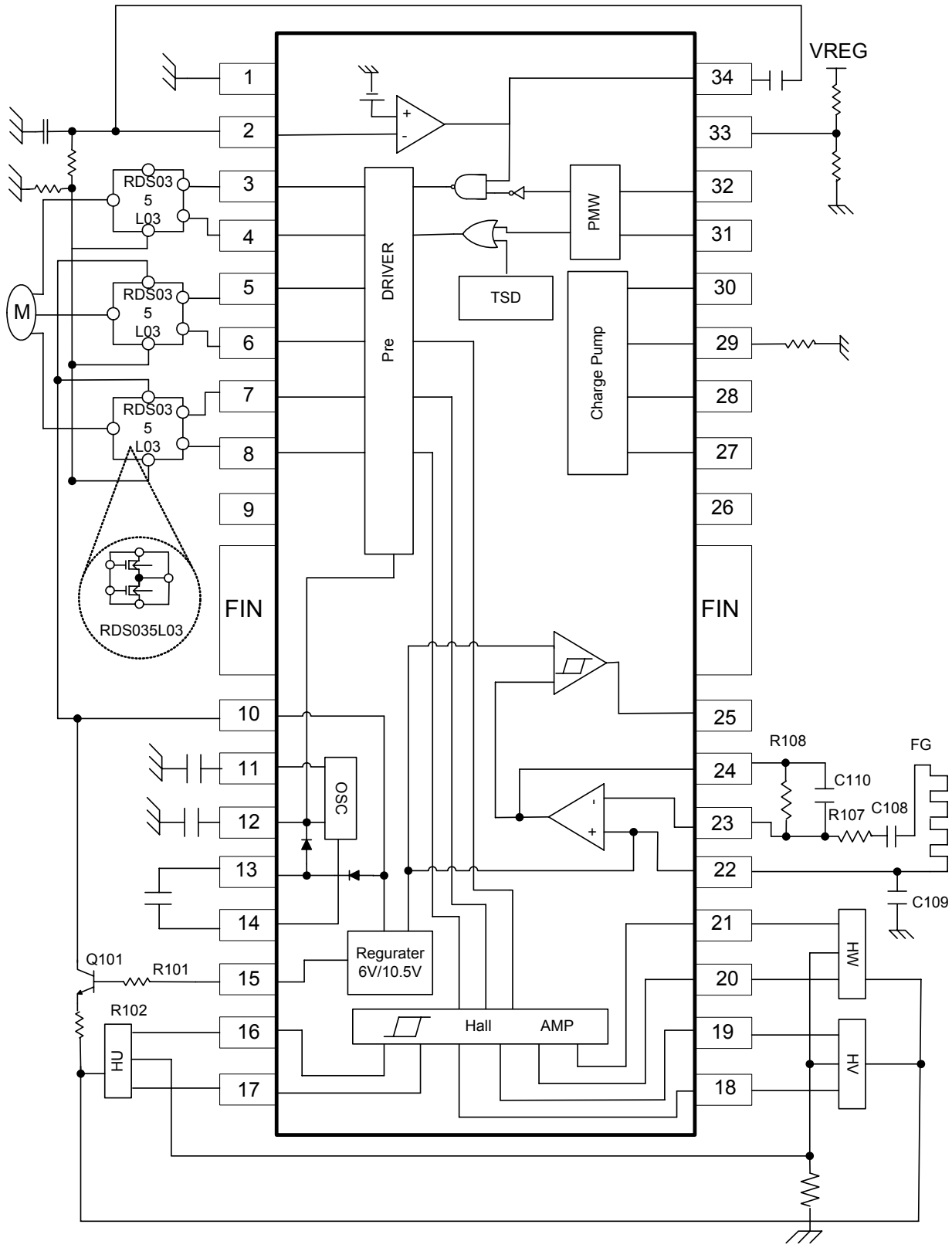
*De-rating is done at 13.6mW/℃ for operating above T_a=25℃

Application circuit

A. F/R rotation circuits



B. Direct PWM Mode circuits



- **Input-Output Table (U = [H], indicates a condition in which $U^+ > U^-$).**

	Input Condition						Output Condition					
							Upper side FET gate Voltage			Lower side FET gate Voltage		
	F/R =H			F/R =L			3	5	7	4	6	8
	U	V	W	U	V	W	UHG	VHG	WHG	ULG	VLG	WLG
Condition 1	L	L	H	H	H	L	L	H	L	L	L	H
Condition 2	L	H	H	H	L	L	H	L	L	L	L	H
Condition 3	L	H	L	H	L	H	H	L	L	L	H	L
Condition 4	H	H	L	L	L	H	L	L	H	L	H	L
Condition 5	H	L	L	L	H	H	L	L	H	H	L	L
Condition 6	H	L	H	L	H	L	L	H	L	H	L	L

Hall input voltage
H:1.3V
M:1.2V
L:1.1V

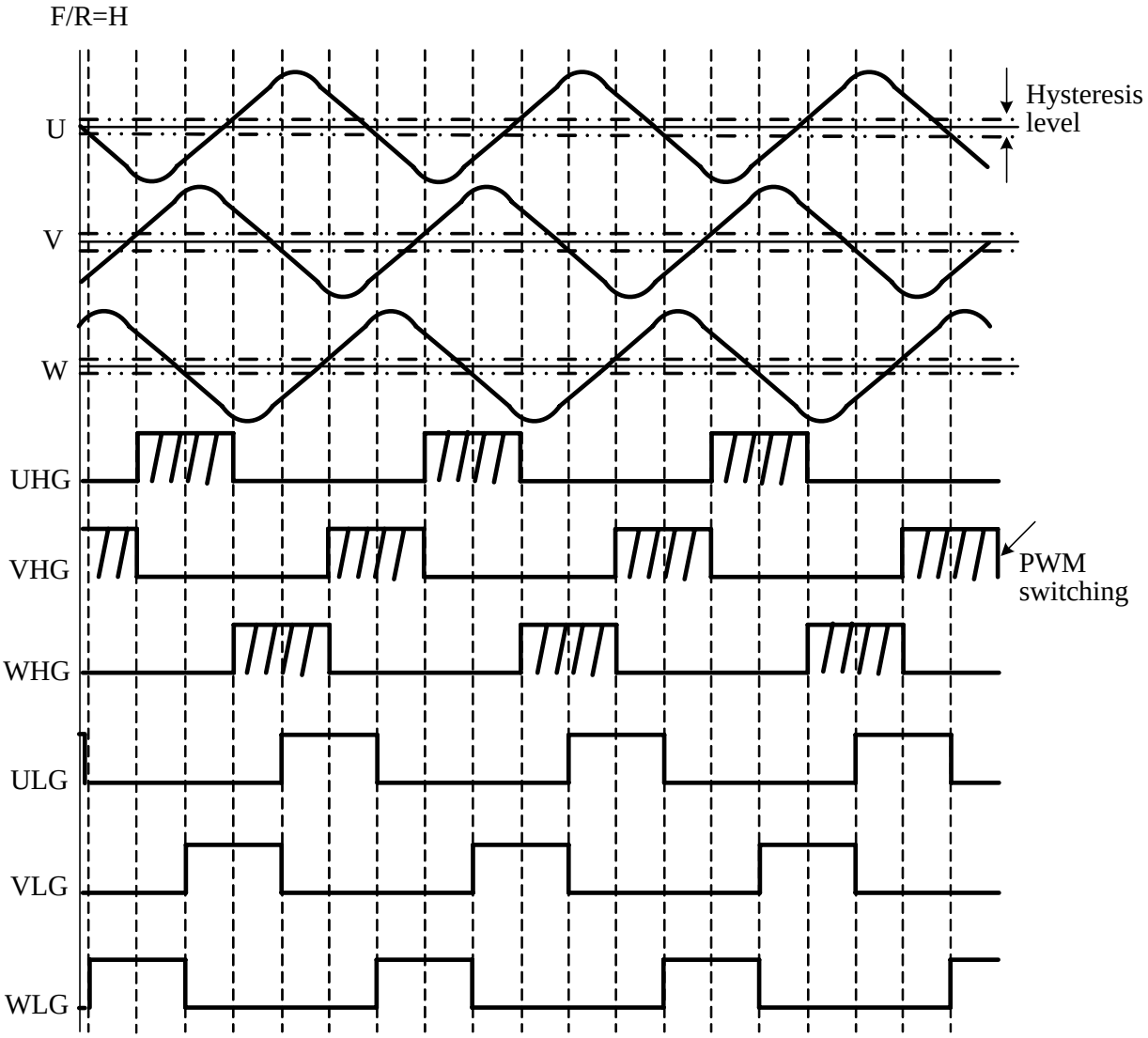
Upper side FET gate voltage
L≦1V , Vb-1V≦H

Lower side FET gate voltage
L≦1V , 9V≦H

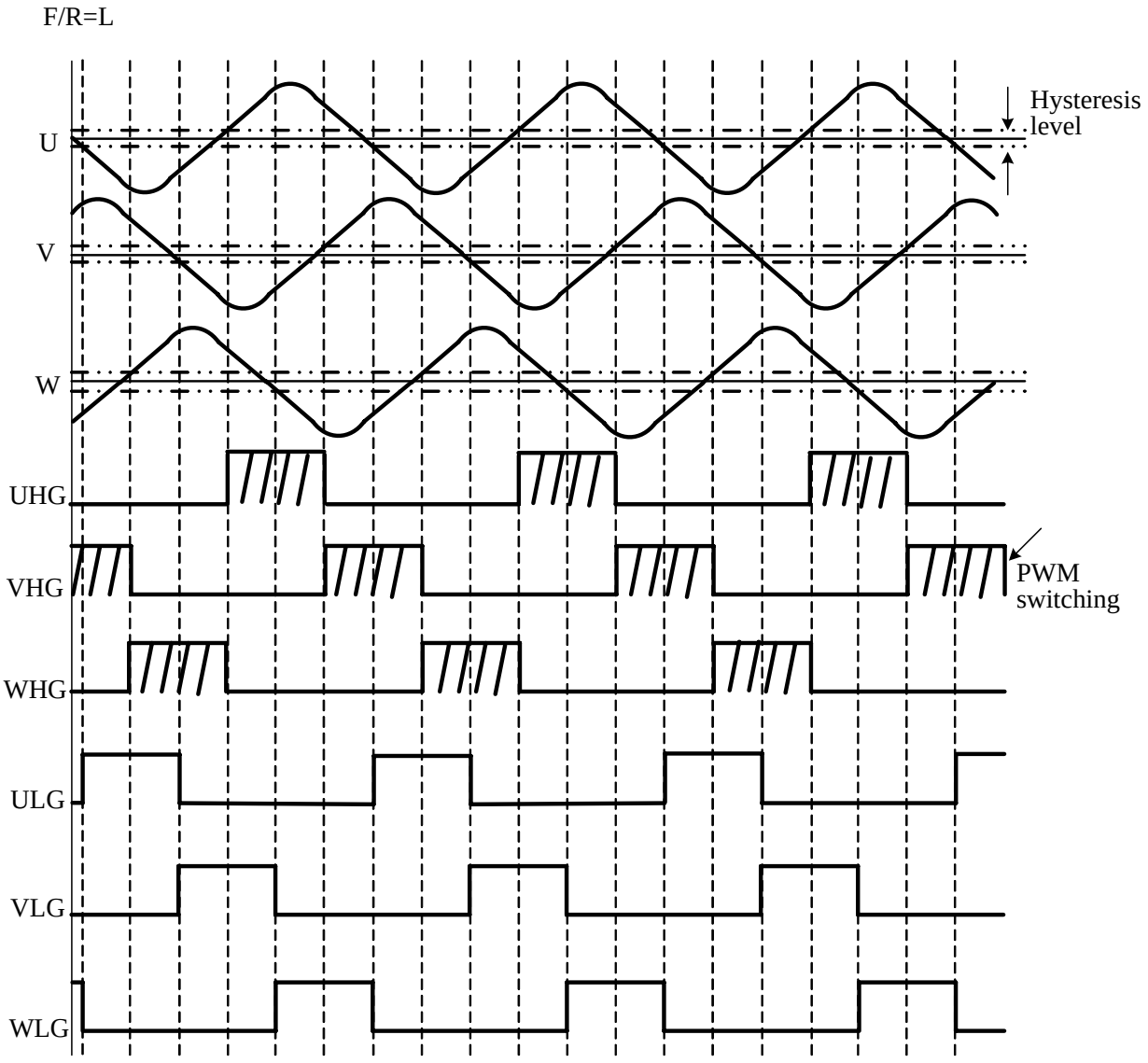
The rotation between F/R input and the motor rotation direction as below:

F/R Input and Motor Rotation	
F/R	Direction
L	U→V→W
H	U→W→V

- **Input-Output timing chart**

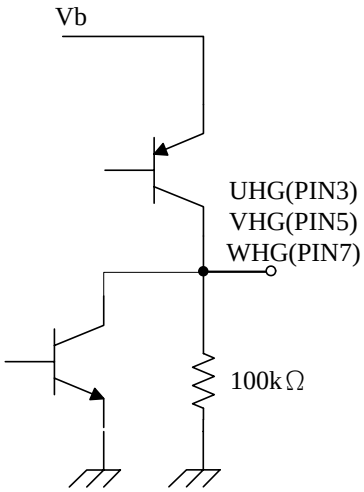


- **Input-Output timing chart**

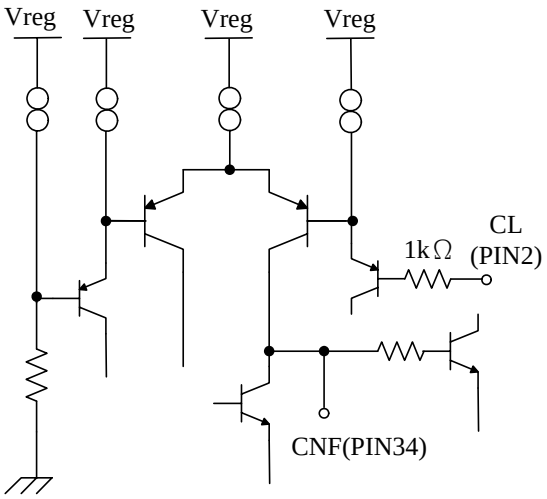


● Input / Output circuit

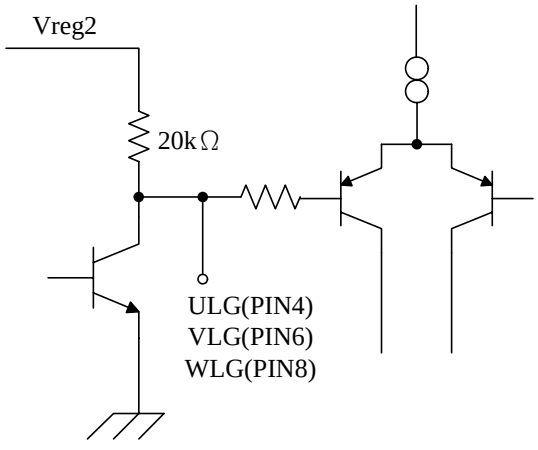
Upper gate



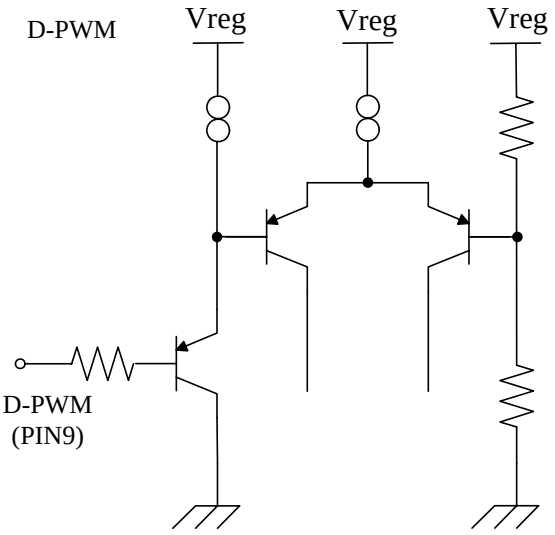
Current limite



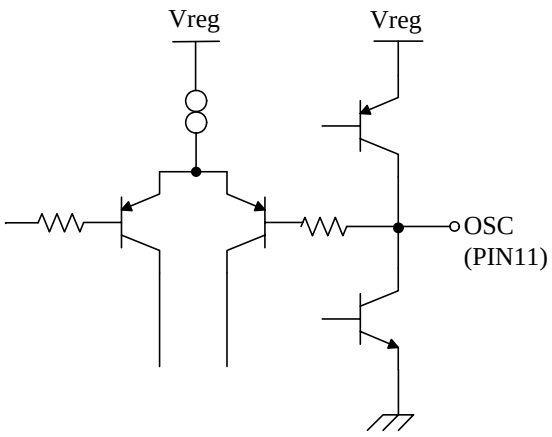
Lower gate



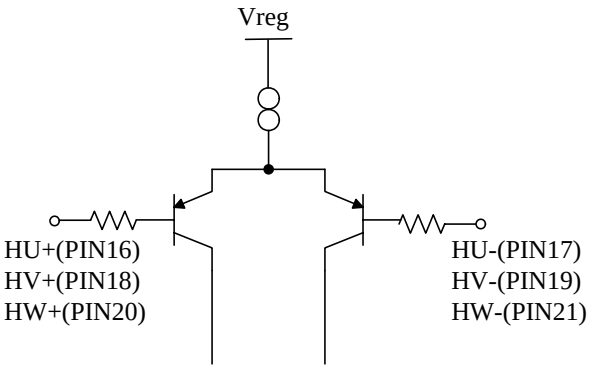
D-PWM



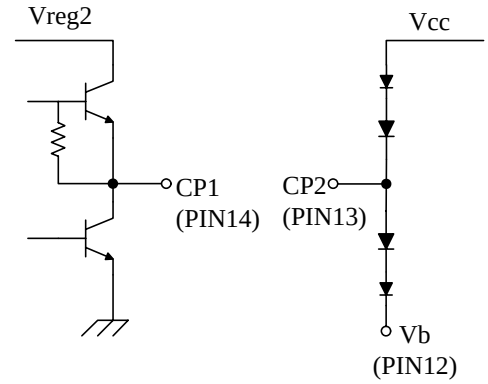
OSC



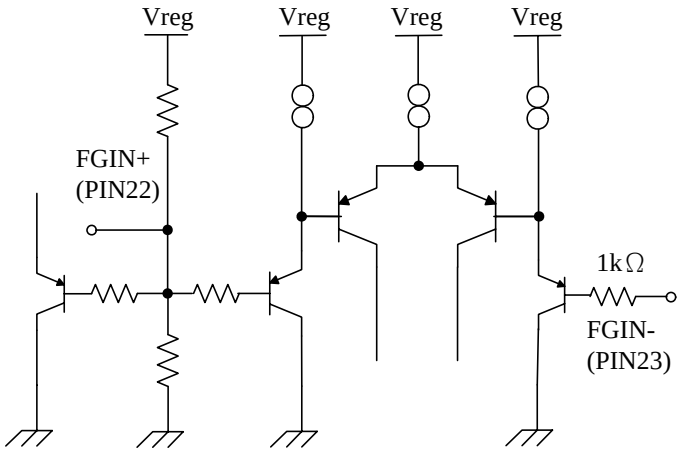
Hall Input



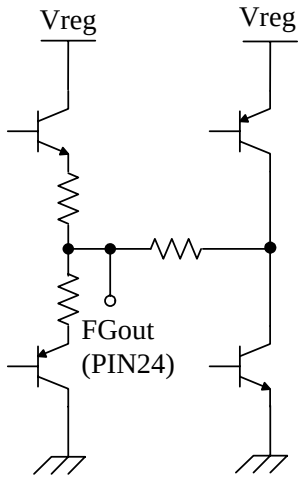
Booster



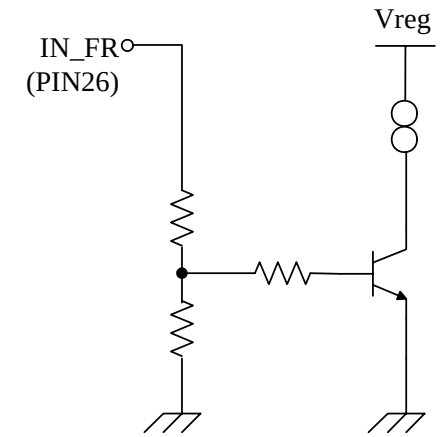
FG Amp Input



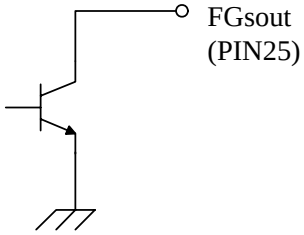
FGout



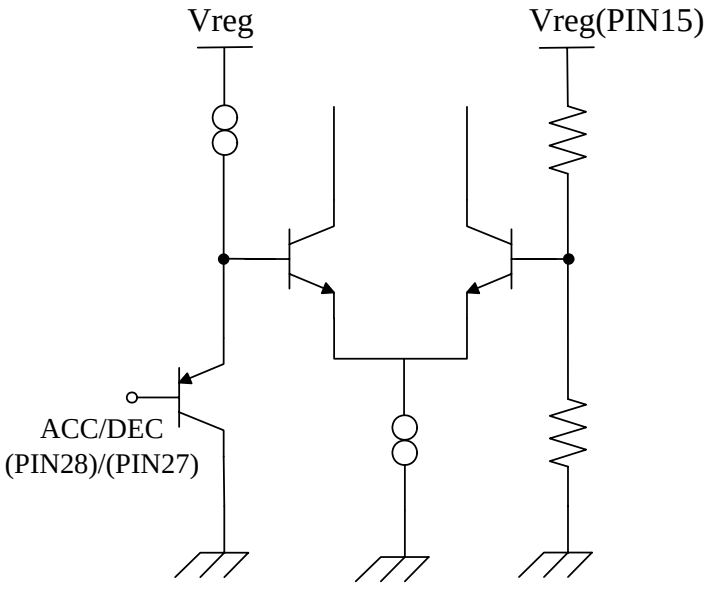
IN_FR PIN



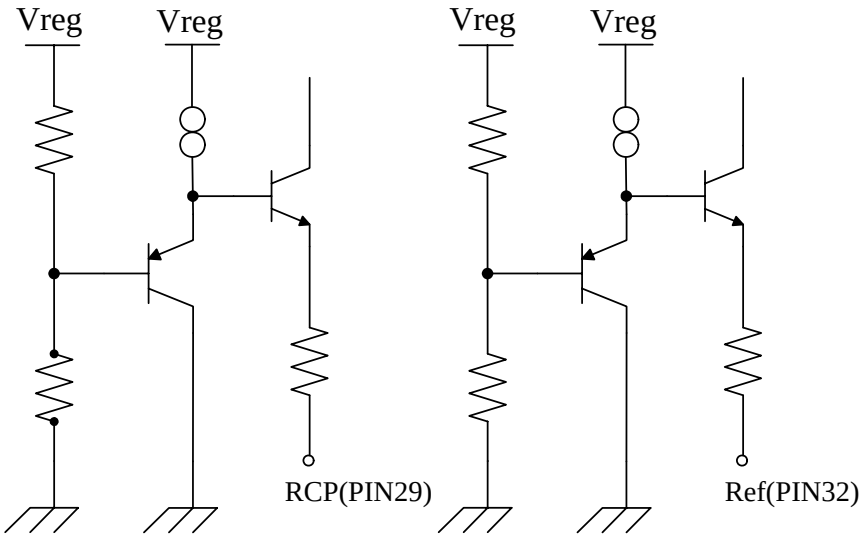
FGsout PIN



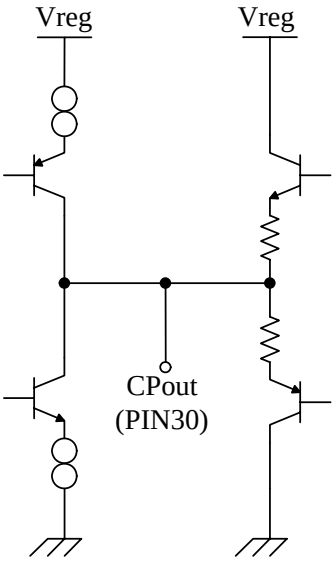
ACC PIN,DEC PIN



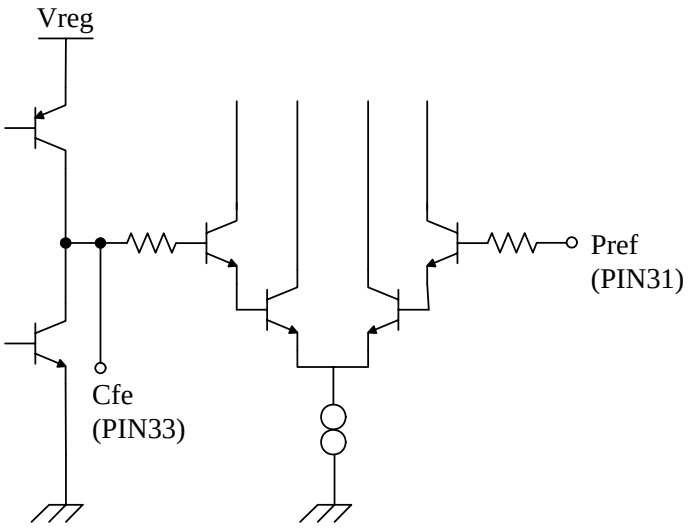
RCP PIN,Rfe PIN



CPout PIN



Compatator Input



Explain of operation

(1) Hall of operation

The signal of Hall Input is arranged at Hall amplifier.

The arranged signal is amplified at pre-driver block, and output a gate voltage of n-ch MOS FET.

(2) PWM operation

By connecting R to Rfe pin and C to Cfe pin, a triangular wave as that shown in Fig.1 generates at Cfe pin.

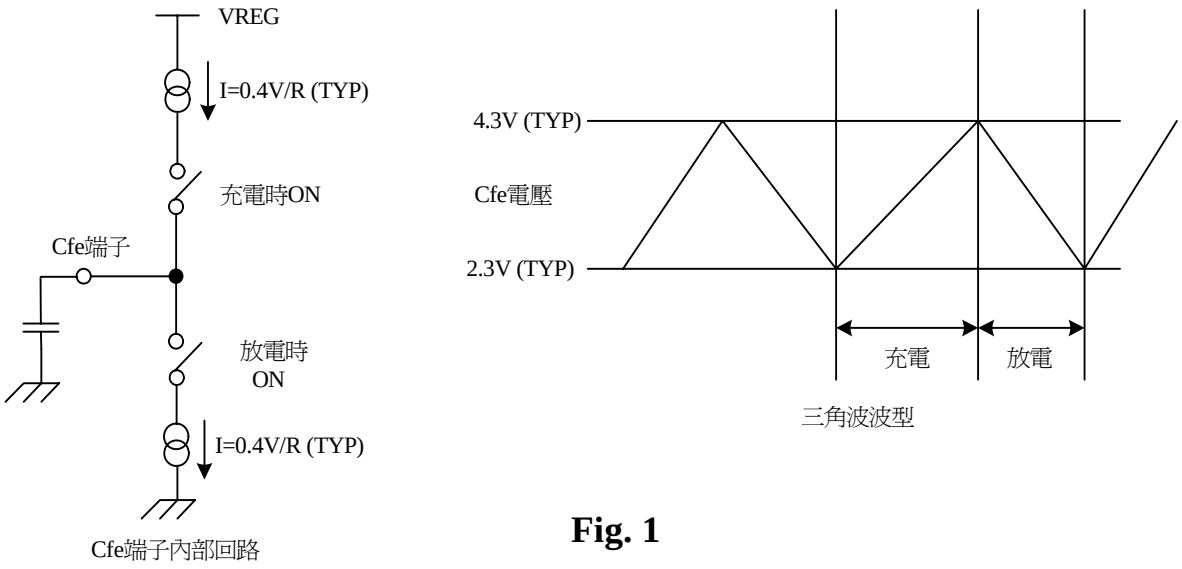


Fig. 1

A frequency of this triangular wave fixes a frequency of PWM.

It is compared that the voltage of the triangular wave and Pref input voltage, drive upper gate voltage of PWM operation.

Parameter table consideration for application:

Spice Simulation.

C	R	Frequency
100pF	51K	17KHz
100pF	45K	20kHz
100pF	38K	25KHz
125pF	36K	20KHz
147pF	36K	17KHz

Fixed C		
C	R	Frequency
100pF	56K	16.4KHz
100pF	51K	17KHz
100pF	43K	20.8KHz
100pF	36K	24.5KHz
100pF	33K	26.5KHz

Fixed R		
C	R	Frequency
120pF	30K	24.2KHz
150pF	30K	19.5KHz
180pF	30K	16.4KHz

(3) Booster

By connecting C to OSC pin, a triangular wave as that shown in Fig.2 generates.

C=100pF: Ferq=250kHz (TYP)

This wave drive CP1, CP2, then a boosted voltage generates.

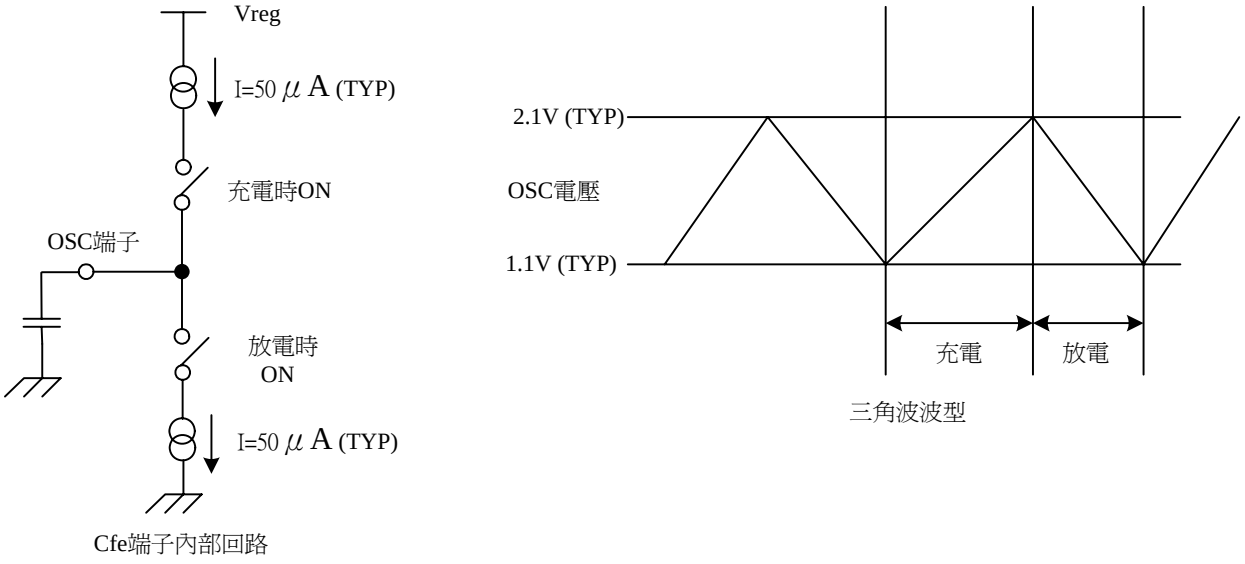


Fig. 2

The boosted voltage, Vb is equal to Vcc+7V (TYP).

SO, please set Vcc, as Vcc+7V is less than absolute maximum voltage.

(4) Current limiter operation

When the CL voltage become 0.38V (TYP), the current limiter circuit activates and limits the PWM ON-Duty. At this time, the output Iomax is limited to:

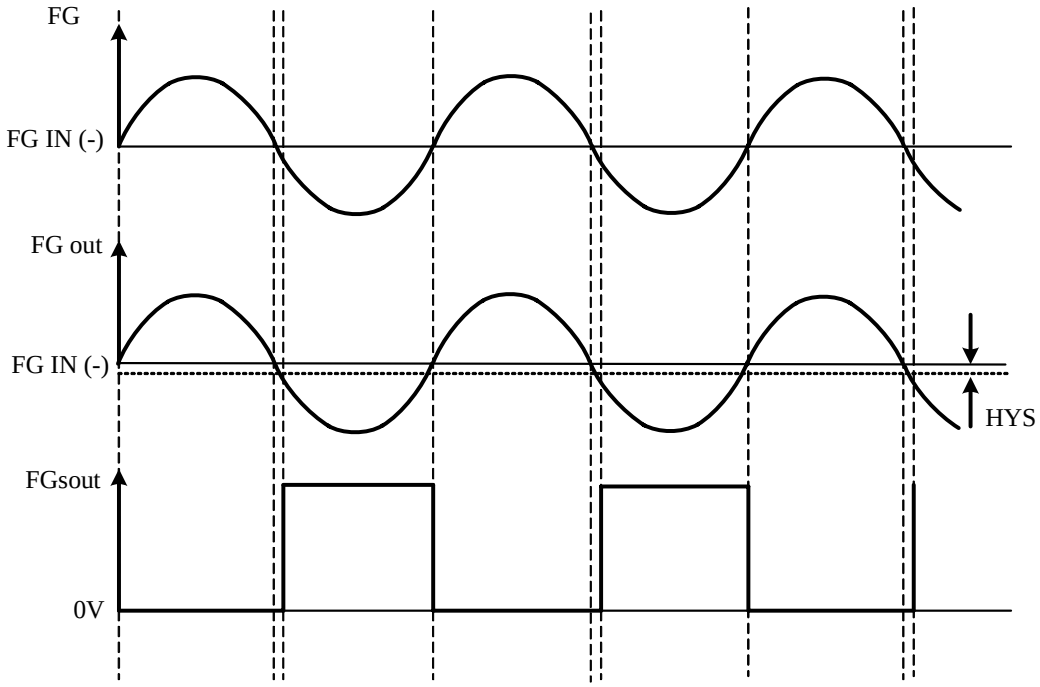
Iomax≒0.38/RNF

(5) FG

FGin+ pin is given 3.0V (TYP) by the inside circuit.

Please set FGamp gain, as FGout voltage stays in Output High, Low voltage, the amplitude is over hysteresis level.

FGout/FGsout timing chart



(6) ACC/DEC

With connecting R to RCP pin, current flow into CPout pin by input Low signal to ACC pin, flow out of CPout pin by input Low signal to DEC pin, By connecting C,R between CPout and GND, this current is changed to voltage.

By connecting CPout pin and Pref pin, and input controlled signal to ACC pin, DEC pin, the Voltage that generated at CPout pin control on-duty of PWM, therefore a motor's rotation is fixed. The truth table is as below:

Note: When RCP ≦ 3.3kΩ, the I-CPout leakage current should be concerned in ACC=HI, DEC=HI situation
RCP = 3.3kΩ ➔ I-CPout leakage current ≒ 220nA at 25℃ (simulation result).

D-PWM/ACC/DEC truth table

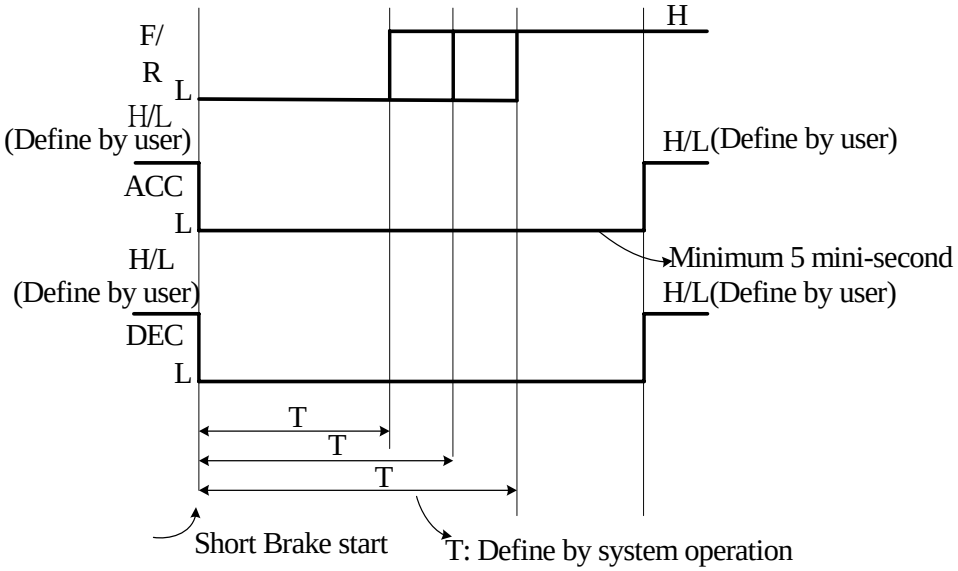
D-PWM	ACC	DEC	CPOUT	function
0	0	0	Y	PWM pulse input, short brake
0	0	1	Y	PWM pulse input
0	1	0	Y	PWM pulse input
0	1	1	Y	PWM pulse input
1	0	0	X	short brake
1	0	1	L	speed up
1	1	0	H	speed down
1	1	1	X	Cap voltage keeps with previous state.

Note: Y means CPout PIN floating.

(7) F/R

It is the motor rotating direction input control pin.

Note: In application with external power N-MOS. It must be set a minimum 5 mini-second short brake delay as motor's rotation from Forward to reverse or reverse to forward to prevent a vertical arm short current which may cause destruction of the external power N-MOS.



(8) D-PWM

Direct PWM mode control pin.

In case “H”：Disable.
In case “L”：Enable.

Note: In application with external power N-MOS. It must be set a minimum 5 mini-second short brake delay as motor’s rotation from Forward to reverse or reverse to forward to prevent a vertical arm short current which may cause destruction of the external power N-MOS.

(9) Under Voltage Protection

When the voltage at Vcc terminal drop to lower than 18.44V (typ), the output of IC will turn off. See the table as below.

Condition A: Vcc＜18.44V

UHG	VHG	WHG	ULG	VLG	WLG
L	L	L	L	L	L

Condition B: Vcc＜18.44V, and ACC/DEC=L

UHG	VHG	WHG	ULG	VLG	WLG
L	H	L	H	L	H

(10) Non-overlap protection

When the voltage of low side motor arises to about 1.5V, the Non-overlap circuit will turn off the high-side motor to prevent short through current. See table as below (Fig.3, Fig.4)

With R= 20Ω Load

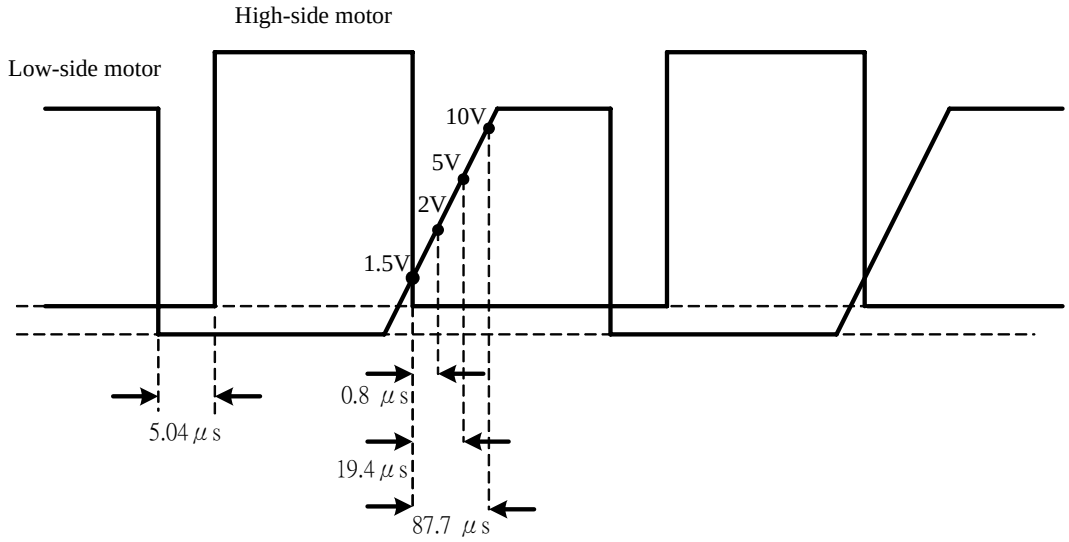


Fig.3

With L=2mH R=2Ω Load

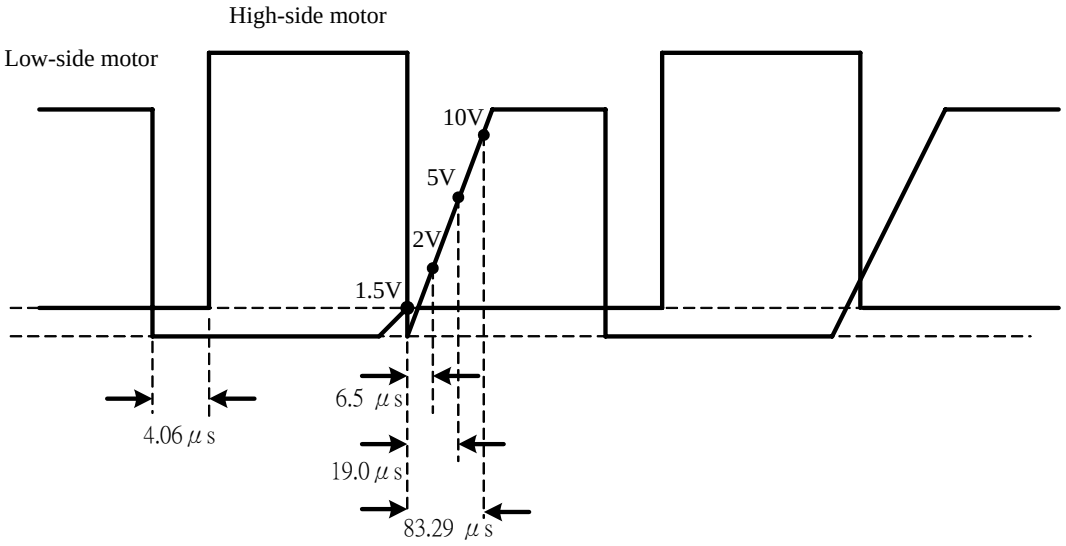
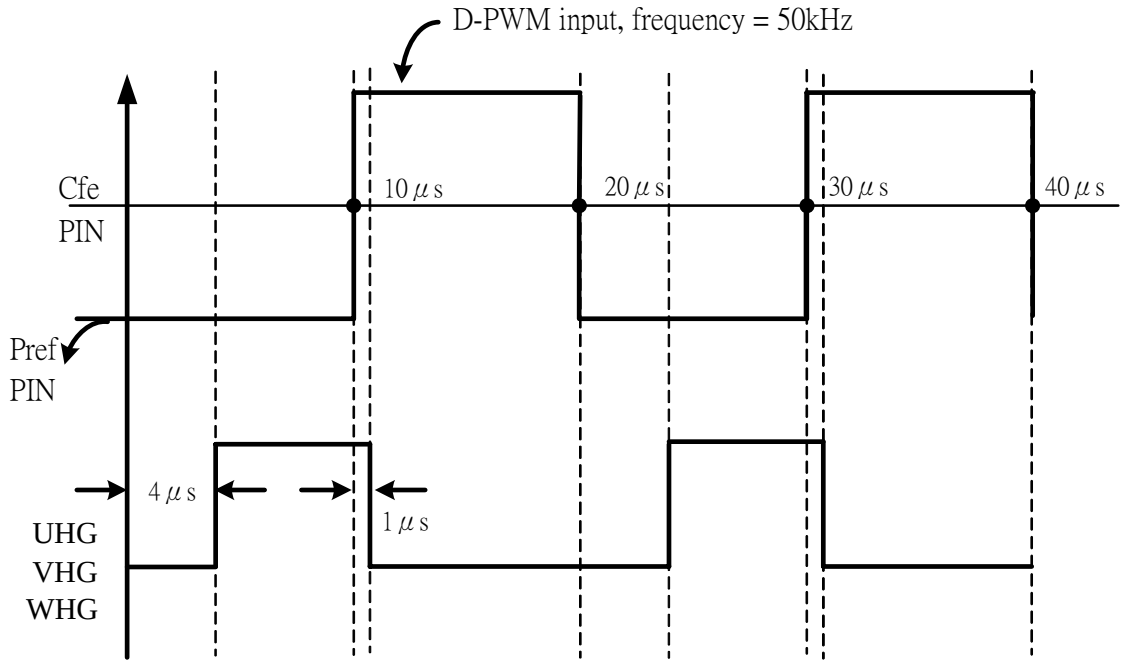


Fig.4

(11) DPWM max frequency chart.



Note :

(1) For stability of a power supply
This IC turns on and off large current of MOS FET by PWM operation
Therefore it is easy to generate a noise inside of this IC
It need to stabilize a line of a power supply.

(2) Show input circuits of Hall Amp to Fig.3
Hall element can be used with both series connection and parallel connection.

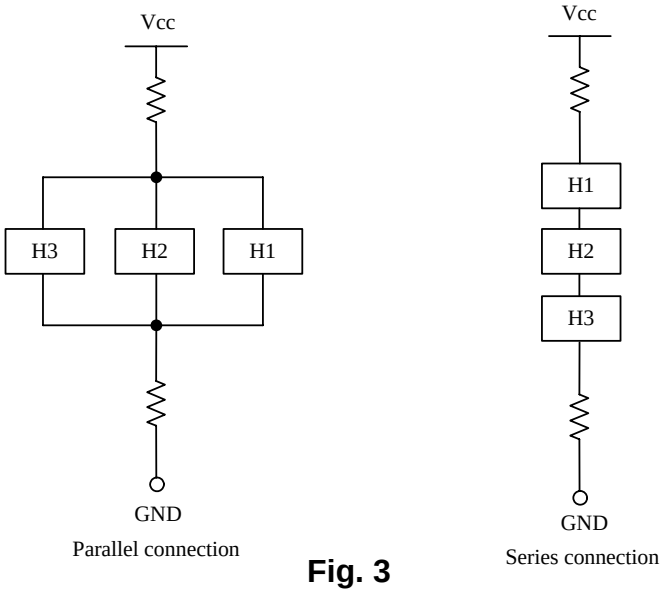


Fig. 3

(3) If the temperature of chip reaches 175℃(TYP), it makes each output goes high impedance and shut down output current. It has the temperature hysteresis of about 25℃(TYP).

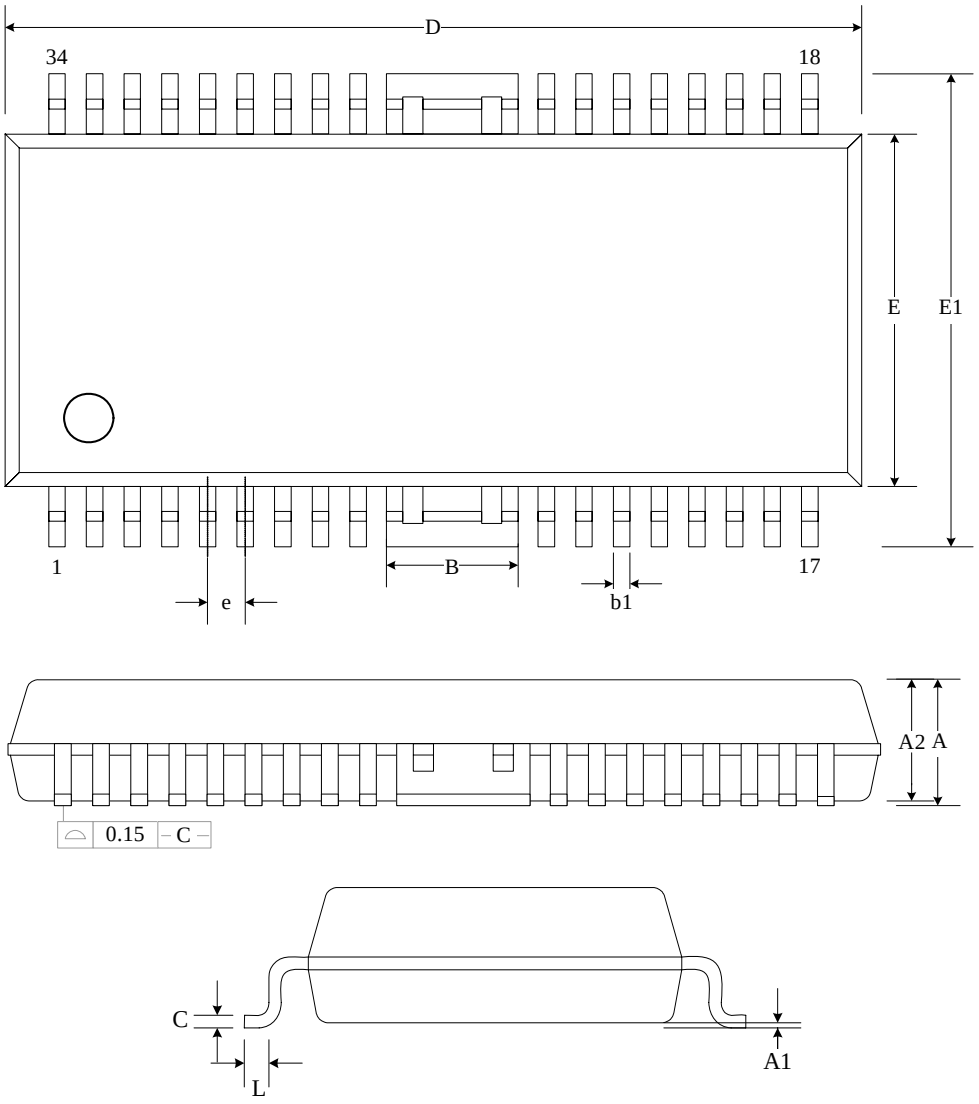
(4) In case used beyond absolute maximum ratings of Gate-Source voltage, in driving at PWM physical security countermeasure, as insert the diode for voltage cramp (order direction : Source → Gate), is to be given.

(5) This product is produced with strict quality control, but it may be destroyed if used beyond absolute maximum ratings. Once IC destroyed, the failure mode cannot be defined (such as short mode, or Open mode). Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

(6) The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics. When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

● Packaging outline

HSOP34



SYMBOL	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	-	2.75	-	0.108
A1	-	0.3	-	0.012
A2	-	2.55	-	0.096
B	2.55	2.95	0.1	0.16
b1	0.23	0.47	0.009	0.019
C	0.2	0.36	0.008	0.014
D	17.89	18.8	0.704	0.740
E	7.3	7.9	0.287	0.311
E1	9.6	10.65	0.378	0.419
e	0.8 (TYP)		0.031(TYP)	
L	0.3	1.27	0.012	0.05

- **Condition of Soldering**

1).Manual Soldering

Pb-free: Time / Temperature ≤ 3 sec / 400 ± 10 °C （2 Times）

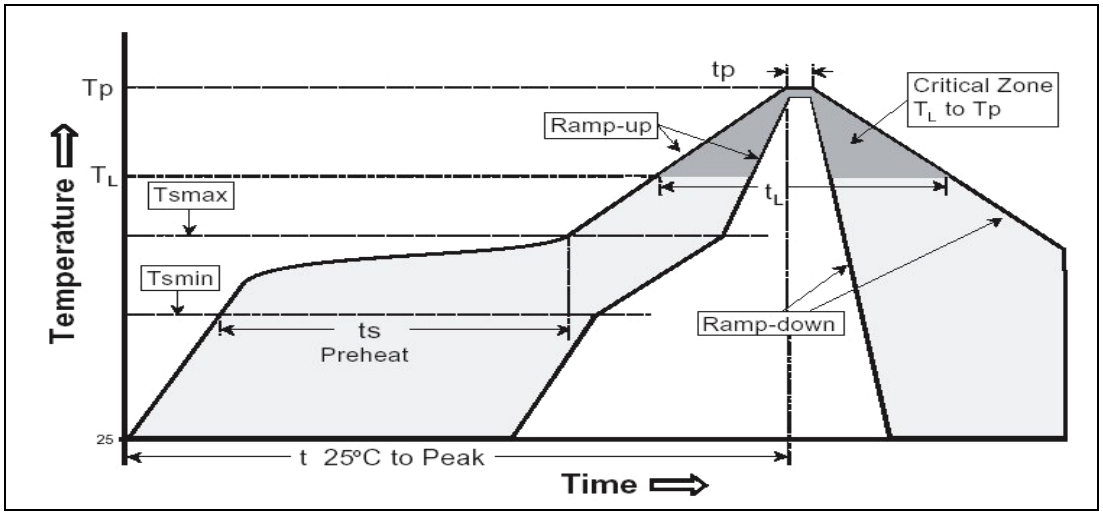
Test Results：0 fail/ 22 tested

Manual Soldering count：2 Times

2).Re-flow Soldering (follow IPC/JEDEC J-STD-020D)

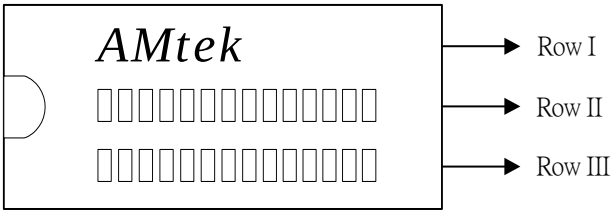
Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.
Preheat - Temperature Min (Ts min) - Temperature Max (Ts max) - Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Ts max to T_L - Temperature Min (Ts min)	 3°C/second max.
Time maintained above: - Temperature (T_L) - Time (t_L)	 217°C 60-150 seconds
Peak Temperature (T_P)	260 +0/-5°C
Time with 5°C of actual Peak - Temperature (tp)	20-40 seconds
Ramp-down Rate	6°C/second max.
Tme 25°C to Peak Temperature	8 minutes max.



- Test Results：0 fail/ 32 tested
- Reflow count：3 cycles

- **Marking Identification**



Row I

AMtek

Row II

AM6807

Row III

Lot number

Note:

V0.33: Change the spec of Vhar, V_{IHD_PWM}, VIHDEC and VIHACC.

V0.35: Change the spec of VCL, VLG and U V W timing chart.

V0.36: Change the ground note of C106, R106 to VREG.

V1.1: Change the FGIN+ connection in application circuit (P9, P10)

V1.2: Add note of I-CPout leakage current concern.